An 802.11 a/b/g/n Digital Fractional-N PLL with Automatic TDC Linearity Calibration for Spur Cancellation

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***Abstract* — This work presents a 1.9~5.6 GHz fractional-N DPLL with digi-phase spur canceller. It utilizes a ramp signal generated from the fractional-N accumulator to automatically calibrate the TDC linearity. The chip also includes an MMD that overcomes the division ration skipping problem associated with the prior art MMDs. The ADPLL achieves a worst fractional spur level of -55 dBc and an in-band phase noise of -109 dBc/Hz (0.63 ps integrated jitter) while consuming 9.9 mW.**

***Index Terms*—DPLL, fractional-N, digi-phase, digital calibration, multi-modulus divider.**

I. Introduction

Digital phase locked loop (DPLL) has advantages of high flexibility for digital calibration that can be utilized to achieve improved performance. A good example is the digi-phase technique [1] which is challenging in an analog PLL due to gain variations in different signal paths, while these gains can be precisely controlled and calibrated in a DPLL [2]. The conventional fractional spur cancellation using sigma-delta modulator (SDM) requires narrow loop bandwidth in order to suppress the noise-shaping component at high frequency band. In addition, SDM also requires a wide range time-to-digital converter (TDC) to cover multiple DCO cycles or another digital-to-time converter (DTC) to reduce the TDC detectable range. Both approaches lead to high power consumption and complexity. These drawbacks motivate us to explore other spur cancellation techniques including digi-phase. Regardless of the techniques employed, the spurious level in DPLL is highly dependent on the linearity of the TDC, necessitating accurate calibrations. In our design, we propose to utilize the ramp signal generated from the fractional-N accumulator to automatically calibrate the TDC linearity and track its gain for precise spur cancellation over process-voltage-temperature (PVT) variations.

This work presents a wideband fractional-N DPLL with digital calibration for fractional spur suppression for a low power Wi-Fi transceiver in 802.11 a/b/g/n bands using a 55 nm CMOS technology. The two-dimensional (2D) Vernier TDC's nonlinearity is automatically calibrated through the fractional frequency synthesis. The implemented RFIC also includes an improved multi-modulus divider (MMD) that overcomes the division ration skipping problem associated with the prior art designs [4].

II. Proposed Architecture

A. *DPLL Architecture*

The proposed DPLL architecture is illustrated in Fig. 1. The digital loop filter consists of proportional and integral paths to achieve a programmable bandwidth from 200 kHz to 2 MHz. Wide loop bandwidth can be employed initially for fast lock. The loop is automatically tuned to an optimal bandwidth that corresponds to the best phase noise performance afterwards. The loop filter generates the frequency control word (FCW) for a wide-tuning digitally controlled oscillator (DCO) running around 3.8~5.6 GHz. Next, a divide-by-2 prescaler divides the 4.8 GHz DCO output to about 2.4 GHz, which allows the DPLL to cover both 2.4 GHz and 5 GHz WiFi bands with only one DCO. An MMD is applied on the feedback path to further scale down the RF frequency with the required ratio. Other DPLLs used high speed counters to replace the MMD [6]. This requires a multi-bits counter running at RF frequency, which is not power efficient. On the other hand, MMD only requires high speed logic at the first stage and the later stages are scaled for lower power consumption as the frequency goes down.

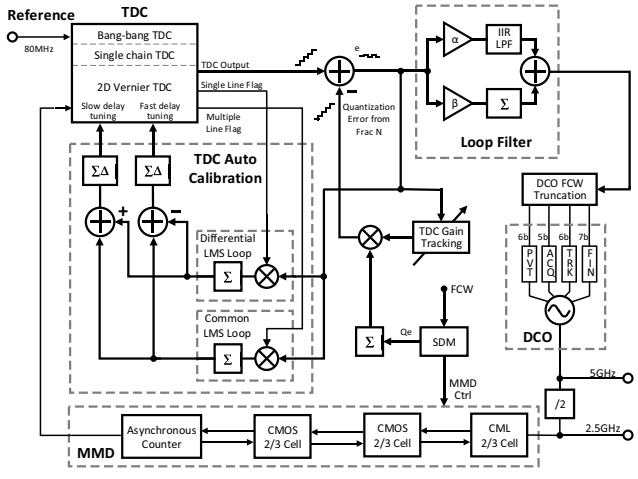

Fig. 1. Proposed DPLL block diagram with automatic TDC linearity calibrations for fractional spur cancellation.

In order to provide a fine resolution over an entire DCO period, the proposed DPLL uses a 2D Vernier TDC with an automatic delay calibration loop for improved linearity. Instead of using a SDM, this design adopts the digi-phase technique in order to suppress the fractional spurs. In the proposed DPLL, the fractional accumulator output (quantization error) is used to generate an inverse stair waveform that is subtracted from the output of the TDC. If the two paths can maintain balanced gains, the injected stair wave can precisely cancel the stair wave at the output of the TDC, leaving only the DC component for frequency tuning, leading to a spur-free fractional operation theoretically. However, implementation of the digi-phase scheme in an analog PLL is challenging due to uncontrollable gains on analog blocks. In order to balance the gains of different feedback paths for this design, a least-mean-square (LMS) loop is utilized to track the TDC gain. With the digi-phase scheme, the fractional spur level is no longer determined by the instantaneous periodic quantization error from the SDM, but is mainly affected by the linearity of the phase discriminator, i.e. the TDC in our case. Thus a highly linear TDC design is critical for the proposed DPLL to achieve superior spectral performance.

B. *Automatic TDC Linearity Calibration*

Due to the detectable range requirement, a 2D Vernier structure [3] was chosen for the TDC as shown in Fig. 2. Similar to the basic Vernier TDC, a fast and a slow delay chains are employed. However, rather than using a single arbiter line, multiple arbiter lines are implemented in a 2D Vernier TDC to compare each delay stage with multiple stages. By re-using part of the delay stages, larger detectable range can be achieved with less hardware compared with a traditional Vernier TDC. However, a highly linear 2D Vernier TDC requires that the delays from both fast and slow chains to satisfy: $n(d_s-d_f)=d_s$, where d_s and d_f denotes delays of a single stage from slow chain and fast chain, n is number of stages in one arbiter line.

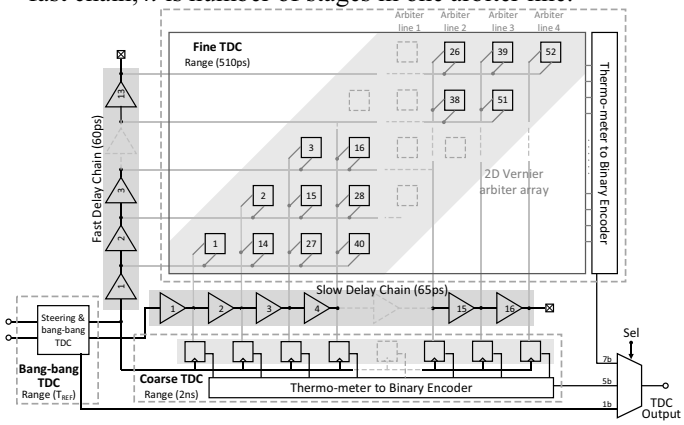

Fig. 2. Segmented TDC including a 2D Vernier fine TDC, a coarse TDC and a bang-bang TDC.

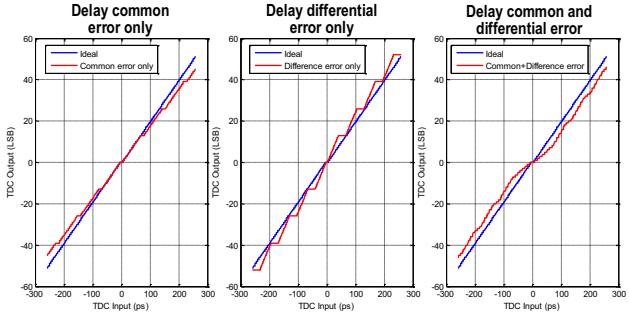

Fig. 3. Simulated TDC non-linearity considering common mode error, differential mode error and both errors, respectively.

As shown in Fig. 3, a common mode error of delays introduces gaps at the turning points of each arbiter line and a differential mode delay error leads to incorrect slope within each line. In this design, we propose to use an automatic calibration procedure for 2D Vernier TDC delay tuning as illustrated in Fig. 1 and can be summarized as follows: Step 1, initially the PLL is locked to a known fractional frequency with digi-phase turned on and TDC gain tracking fixed at a pre-set value. Step 2, after lock-in, TDC calibration utilizes the ramp signal at the TDC output for TDC delay calibration. Step 3, turn off delay calibration, turn on TDC gain tracking and relock to the desired frequency.

With a closer look, the quantization error generated by the factional-N accumulator shows a staircase ramp waveform that can be used to sweep the TDC input from $-T_{DCO}/2$ to $T_{DCO}/2$. The corresponding TDC output is further subtracted from an ideal ramp signal, creating an error signal that is used to automatically adjust the TDC delays. As mentioned above, when TDC input is within the range of first arbiter line, only the difference between fast and slow delays causes TDC measurement error. On the other hand, the average of fast and slow delays dominates TDC error when TDC input is so large such that multiple arbiter lines are used. As a result, the common and differential parts of the fast and slow delays can be calibrated separately according to TDC's input range. Two LMS loops are designed to collect the differential and common error signals used for fast and slow delay calibrations. The difference LMS loop is enabled when only the first arbiter line is activated and the common LMS loop is enabled when multiple arbiter lines are activated. In this way, we can guarantee an orthogonal calibration of two types of errors without interfering with each other. With auto-calibration, this 2D Vernier TDC achieves an average DNL of 1.13 LSB and INL of 0.81 LSB, while DNL and INL are 1.32 LSB and 3.49 LSB without calibration, respectively. The DNL is mainly caused by the 2D arbiter topology, where the turning points of the arbiter chains correspond to worst DNL. The proposed TDC gain and linearity calibration only needs to be carried out once initially and involves negligible extra power consumption.

III. Circuit Implementation

A. *2D Vernier TDC*

In order to achieve a fine resolution and large detectable range, the TDC adopts a segmented architecture constructed with 3 sub-TDCs as shown in Fig. 2. The finest TDC is a Vernier TDC with 2D arbiter array [3] that achieves a fine resolution of 5ps. This fine TDC has a detectable range of 510 ps (7 bits), sufficient to cover an entire DCO cycle. The 2^{nd} sub-TDC reuses the slow delay chain of the Vernier TDC to provide a non-Vernier measurement with a coarse resolution of 65 ps and a detectable range up to 2 ns (5 bits). Beyond this range, a 3rd bang-bang TDC is applied to provide lag or lead information for a wide detectable range. Note that the 2nd sub-TDC causes neither extra hardware nor power. Moreover, the 2D Vernier TDC can utilize the difference between two delay chains to balance PVT variations. As mentioned before, only a specific pair of fast and slow delays results in the best linearity (60 ps and 65 ps in this case). To provide the accuracy needed for digital calibration, both delays are adjustable with 6-bit control and 0.5 ps step size. In addition, a first order sigma-delta modulator was added at delay control input to further improve TDC delay tuning accuracy.

B. *Wide-tuning DCO*

As shown in Fig. 4, the wide tuning DCO consists of 4 frequency banks: fine bank (FIN), track bank (TRK), acquisition bank (ACQ) and PVT bank. With a divide-by-2 for generating the 2.4 GHz band, this DPLL is able to cover 1.9~2.8 GHz and 3.8~5.6 GHz bands for multi-band applications. Thus, the DCO is equipped with a wide-tuning range of 35%. The PVT bank of the DCO consists of 6 binary bits to pre-set the DCO tuning word for fast locking. The system will first use a successive approximation (SAR) algorithm to search for the PVT code for a desired frequency tuning word. The finest bank has 7 thermometer coded bits with a frequency resolution of 15 kHz/step to minimize the DCO quantization noise. Two fixed capacitors are connected in series with the capacitor array to shrink the frequency tuning step.

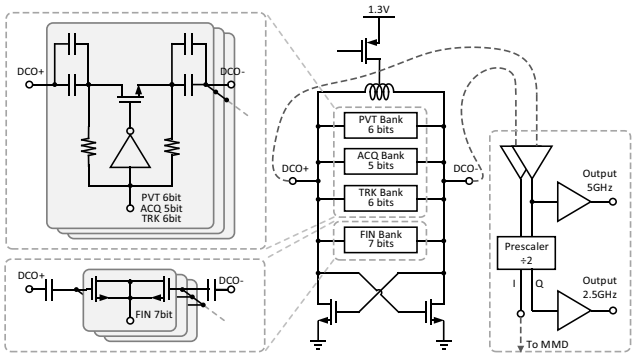

Fig. 4. The wide-tuning DCO with 4 capacitor banks.

C. *Error-Free Multi-Modulus Divider*

Conventional MMD uses additional logic to achieve the extended division range from 2^m to 2^{n-1} [4]. However, the architecture presents a hidden problem with wrong division ratio in the first cycle when it toggles across a division ratio of 2's power. The source for this error lies upon the fact that additional division cells are activated when division ratio toggles across the border between extended and non-extended stages. As shown in Fig. 5, the extension cells can be in a random state when activated, leading to incorrect divider output. Division ratio dependent solutions have been proposed for limited extension bits [4], but extending to higher bits still remains non-trivial. To tackle this problem, we propose to use a single synthesizable state machine to replace all the stages with ratio extension logics. This new MMD uses an asynchronous counter to count the divided edges from previous stages which essentially served the same purpose as those replaced stages. Moreover, the counter is locked to a known state when disabled, thus it will propagate correct modular control signal through the divide-by-2/3 chain when enabled. A division range programmable from 8 to 127 is achieved with no division ratio switching error. The wide programmable division ratio enables the wide-tuning capability for this DPLL. The additional digital circuit is clocked by the divided DCO clock around 300 MHz and costs ignorable overhead in terms of power and area. The 3 LSBs of MMD division control drive conventional 2/3 cells, while the 4 MSBs are implemented with the asynchronous counter.

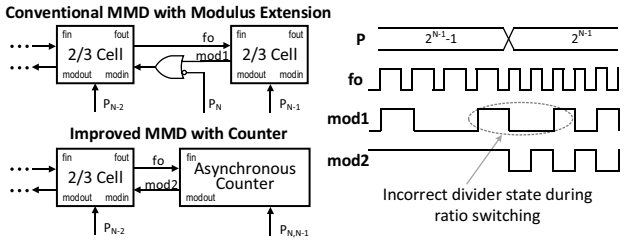

Fig. 5. Improved MMD structure with no ratio switching error.

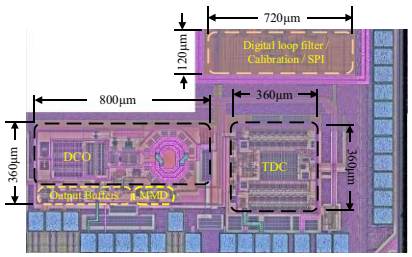

Fig. 6. Die photo of the DPLL for a low power multi-standard wireless transceiver.

IV. Measurement Results

This design was fabricated in a 55nm CMOS technology as part of a low power multi-standard wireless transceiver.

The ADPLL occupies an area of 0.56 mm^2 as shown in the die photo of Fig. 6. The loop bandwidth is tuneable from 200 kHz to 2 MHz. With the bandwidth set to 2 MHz, the measured in-band phase noise was -109 dBc/Hz and the integrated *rms* jitter was 0.63 ps as shown in Fig. 7. The in-band spur is due to the power regulator used on board. The DPLL uses an off-chip 80 MHz crystal oscillator as the reference. The chip consumes 9.9 mW total power in which TDC, DCO and the digital circuits (including MMD) consumes 4.7 mW, 4.2 mW and 1 mW, respectively.

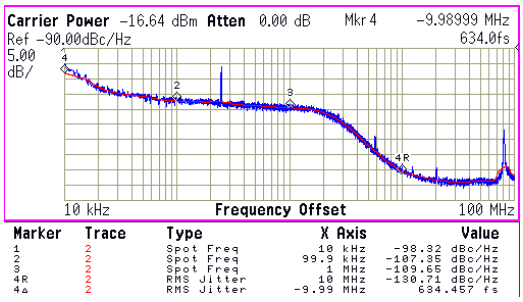

Fig. 7. Measured phase noise at 2.08 GHz output with loop bandwidth of 2 MHz.

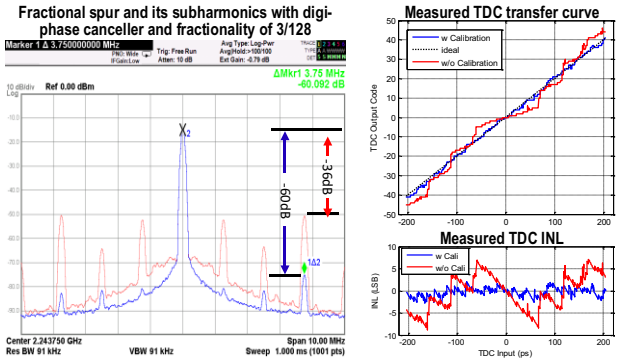

Fig. 8. Measured performance before and after digital calibration.

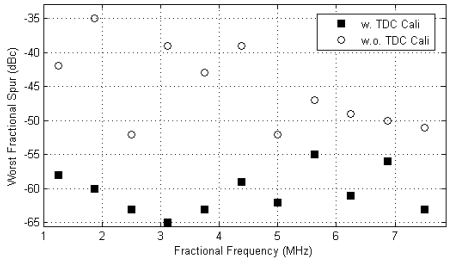

Fig. 9. Measured fractional spur near 2.4 GHz with a loop bandwidth of 2 MHz for different fractional frequencies with and without TDC calibrations.

As shown in Fig. 8 with fractionality of 3/128, the DPLL with digi-phase presents the worst spur level of -35 dBc at 3.75 MHz offset in companion with its subharmonic spurs due to TDC nonlinearity before the TDC calibration. When the TDC is calibrated, fractional spurs drops below -60 dBc, indicating a spur reduction of 25 dB owing to the proposed digital calibration technique. The worst fractional spurs measured near 2.4 GHz with various fractional frequencies are shown in Fig. 9 showing the effectiveness of TDC calibration for spur reduction. Performance comparisons are summarized in table 1, demonstrating a competitive DPLL design among the state-of-the-art.

TABLE.1 MEASURED DPLL PERFORMANCES AND COMPARISONS.

	Hsu [6] ISSCC08	Gao [7] ISSCC15	Zanuso [2] JSSC11	This work
Technology	130nm	28nm	65nm	55nm
References (MHz)	50	80	40	80
Output frequency (GHz)	3.2-4.2	5.8	3.0-3.6	1.9~2.8/ 3.8~5.6
Tuning range (%)	27.2	/	18.2	32.1*
In-band PN (dBc/Hz)	-108	-105	-104	-109
Worst fractional spur (dBc)	-42	/	-57	-55
RMS jitter (fs) **	204	173	893	634
RMS PN (deg) **	0.27	0.36	1.15	0.46
TDC resolution (ps)	6	/	4	5
DCO resolution (kHz/bit)	/	100	0.04	15
Power (mW)	46.7	9.5	80	9.9
Core area (mm^2)	0.95	0.3	0.4	0.56

* Measured for each band, ** integrated from 10 kHz to 10 MHz.

V. CONCLUSIONS

This paper presented an ADPLL covering 1.9~5.6 GHz band. By using a ramp signal generated from fractional frequency synthesis, the loop can automatically adjust TDC's fast and slow delays to achieve the best linearity for fractional spur reduction. Furthermore, the improved MMD structure provides a wide tuning division range from 8~127 without transient switching error to support the required wide DCO tuning range of 35%.

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